



**256K x 36, 512K x 18**  
**3.3V Synchronous ZBT™ SRAMs**  
**ZBT™ Feature**  
**3.3V I/O, Burst Counter**  
**Pipelined Outputs**

**AS8C803601**  
**AS8C801801**

**Features**

- ◆ 256K x 36, 512K x 18 memory configurations
- ◆ Supports high performance system speed - 150MHz (3.8ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control  $\overline{OE}$
- ◆ Single  $R/\overline{W}$  (READ/WRITE) control pin
- ◆ Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- ◆ 4-word burst capability (interleaved or linear)
- ◆ Individual byte write ( $\overline{BW}_1$  -  $\overline{BW}_4$ ) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 3.3V power supply ( $\pm 5\%$ )
- ◆ 3.3V I/O Supply ( $V_{DDQ}$ )
- ◆ Power down controlled by ZZ input
- ◆ Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP).

**Description**

The AS8C803601/801801 are 3.3V high-speed 9,437,184 bit (9 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The AS8C803601/801801 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ( $\overline{CEN}$ ) pin allows operation of the AS8C803601/801801 to be suspended as long as necessary. All synchronous inputs are ignored when ( $\overline{CEN}$ ) is high and the internal device registers will hold their previous values.

There are three chip enable pins ( $\overline{CE}_1, \overline{CE}_2, \overline{CE}_2$ ) that allow the user to deselect the device when desired. If anyone of these three are not asserted when  $\overline{ADVLD}$  is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The AS8C803601/801801 have an on-chip burst counter. In the burst mode, the AS8C803601/801801 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the  $\overline{LBO}$  input pin. The  $\overline{LBO}$  pin selects between linear and interleaved burst sequence. The  $\overline{ADVLD}$  signal is used to load a new external address ( $\overline{ADVLD} = \text{LOW}$ ) or increment the internal burst counter ( $\overline{ADVLD} = \text{HIGH}$ ).

The AS8C803601/801801 SRAM utilize IDT's latest high-performance CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP).

**Pin Description Summary**

A <sub>0</sub> -A <sub>18</sub>	Address Inputs	Input	Synchronous
$\overline{CE}_1, \overline{CE}_2, \overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$R/\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1, \overline{BW}_2, \overline{BW}_3, \overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADVLD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Asynchronous
I/O <sub>0</sub> -I/O <sub>31</sub> , I/OP <sub>1</sub> -I/OP <sub>4</sub>	Data Input / Output	I/O	Synchronous
V <sub>DD</sub> , V <sub>DDQ</sub>	Core Power, I/O Power	Supply	Static
V <sub>SS</sub>	Ground	Supply	Static

5304 tbi 01

## Pin Definitions<sup>(1)</sup>

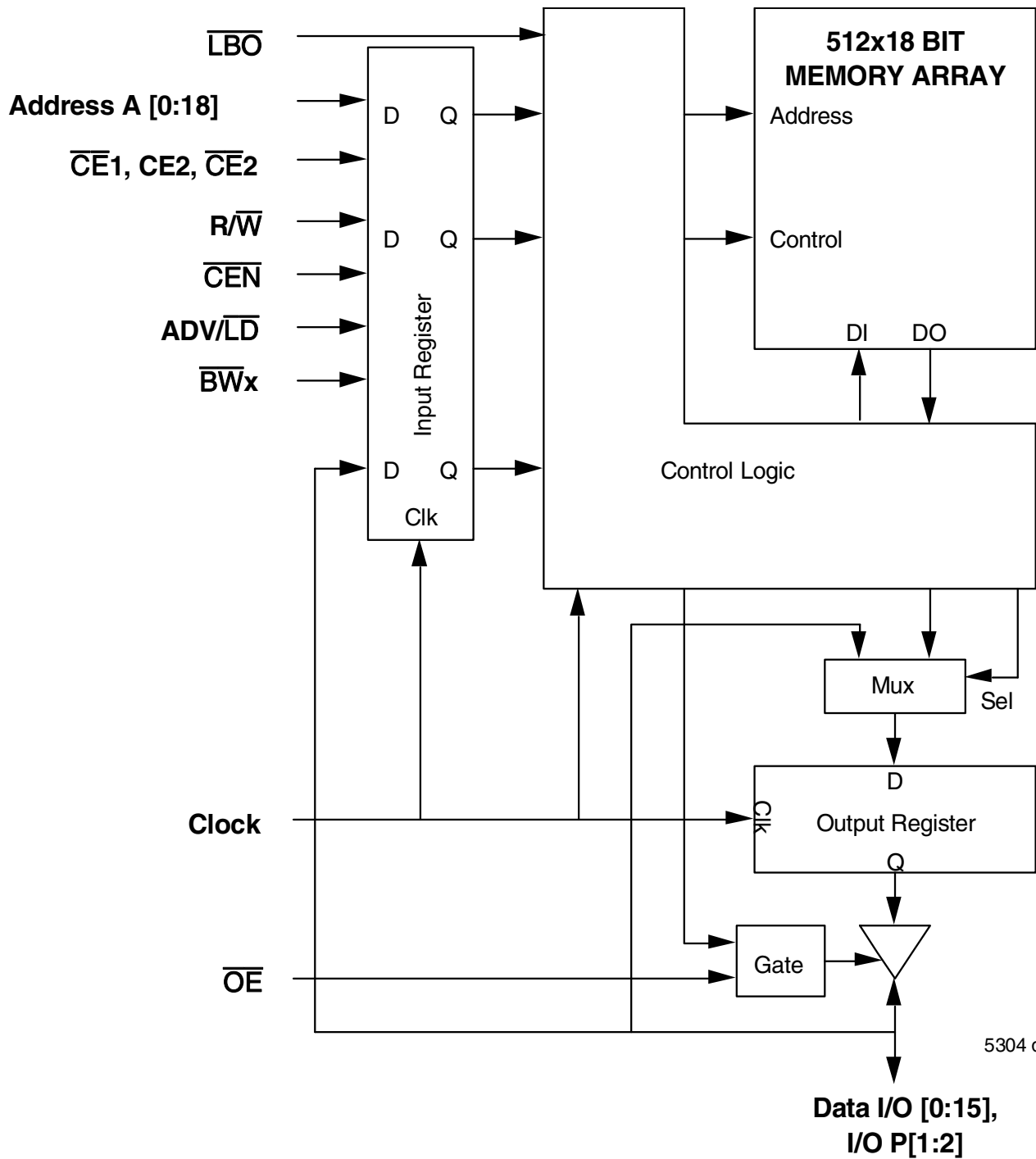
Symbol	Pin Function	I/O	Active	Description
A <sub>0</sub> -A <sub>18</sub>	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, CEN low, and true chip enables.
ADV/LD	Advance / Load	I	N/A	ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.
R/W	Read / Write	I	N/A	R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
CEN	Clock Enable	I	LOW	Synchronous Clock Enable Input. When CEN is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CEN sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, CEN must be sampled low at rising edge of clock.
BW <sub>1</sub> -BW <sub>4</sub>	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal (BW <sub>1</sub> -BW <sub>4</sub> ) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BW <sub>1</sub> -BW <sub>4</sub> can all be tied low if always doing write to the entire 36-bit word.
CE <sub>1</sub> , CE <sub>2</sub>	Chip Enables	I	LOW	Synchronous active low chip enable. CE <sub>1</sub> and CE <sub>2</sub> are used with CE <sub>2</sub> to enable the AS8C803601/801801 (CE <sub>1</sub> or CE <sub>2</sub> sampled high or CE <sub>2</sub> sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE <sub>2</sub>	Chip Enable	I	HIGH	Synchronous active high chip enable. CE <sub>2</sub> is used with CE <sub>1</sub> and CE <sub>2</sub> to enable the chip. CE <sub>2</sub> has inverted polarity but otherwise identical to CE <sub>1</sub> and CE <sub>2</sub> .
CLK	Clock	I	N/A	This is the clock input to the AS8C803601/801801. Except for OE, all timing references for the device are made with respect to the rising edge of CLK.
I/O <sub>0</sub> -I/O <sub>31</sub> I/O <sub>P1</sub> -I/O <sub>P4</sub>	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
LBO	Linear Burst Order	I	LOW	Burst order selection input. When LBO is high the Interleaved burst sequence is selected. When LBO is low the Linear burst sequence is selected. LBO is a static input and it must not change during device operation.
OE	Output Enable	I	LOW	Asynchronous output enable. OE must be low to read data from the AS8C803601/801801. When OE is high the I/O pins are in a high-impedance state. OE does not need to be actively controlled for read and write cycles. In normal operation, OE can be tied low.
ZZ	Sleep Mode	I	N/A	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the AS8C803601/801801 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.
V <sub>DD</sub>	Power Supply	N/A	N/A	3.3V core power supply.
V <sub>DDQ</sub>	Power Supply	N/A	N/A	3.3V I/O Supply.
V <sub>SS</sub>	Ground	N/A	N/A	Ground.

**NOTE:**

5304tbl 02

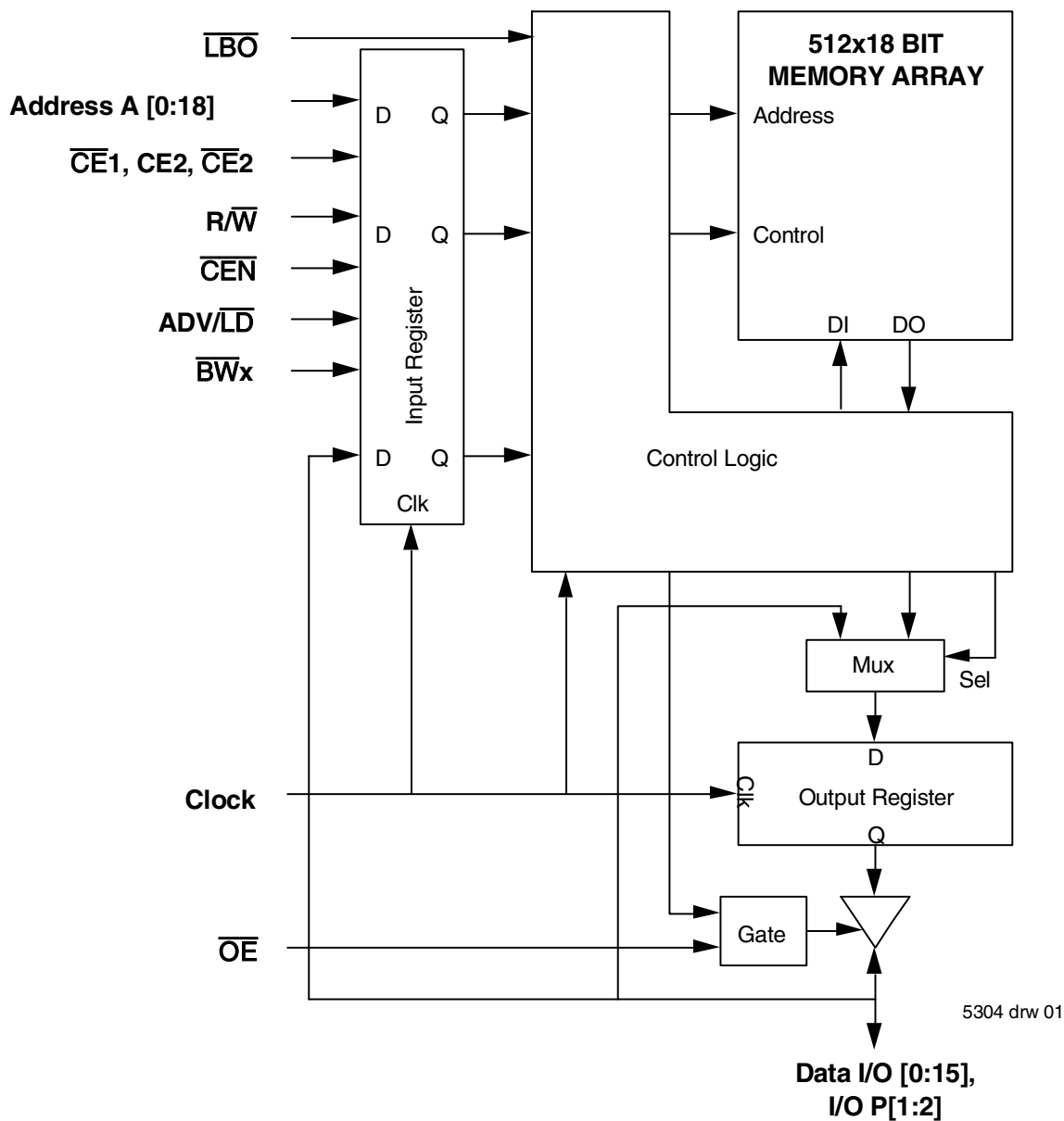
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

# Functional Block Diagram



5304 drw 01

## Functional Block Diagram



5304 drw 01

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.135	3.3	3.465	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.135	3.3	3.465	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage - Inputs	2.0	—	V <sub>DD</sub> +0.3	V
V <sub>IH</sub>	Input High Voltage - I/O	2.0	—	V <sub>DDQ</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

5304 tbl 04

### NOTES:

- V<sub>IL</sub> (min.) = -1.0V for pulse width less than t<sub>cyc</sub>/2, once per cycle.

# Recommended Operating Temperature and Supply Voltage

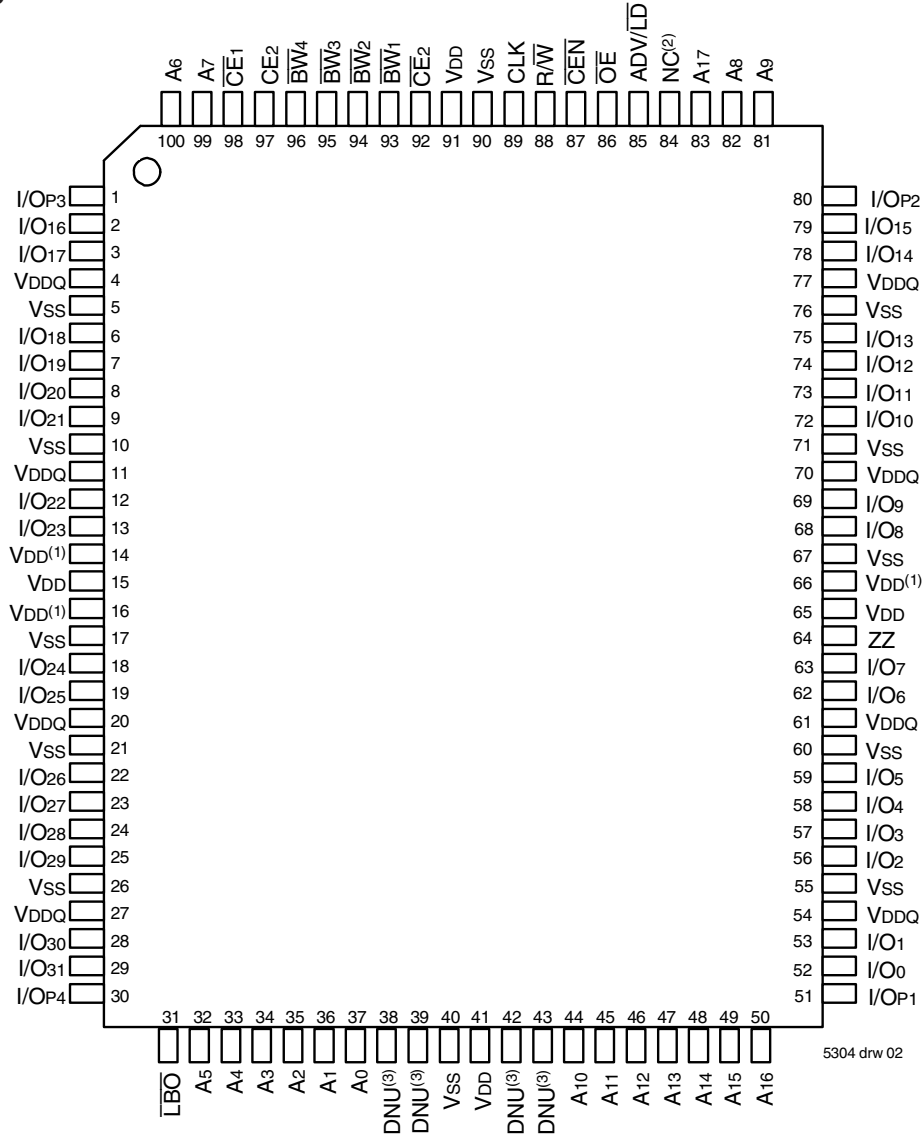
Grade	Ambient Temperature <sup>(1)</sup>	Vss	VDD	VDDQ
Commercial	0° C to +70° C	0V	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	3.3V±5%

**NOTES:**

5304 tbl 05

1. During production testing, the case temperature equals the ambient temperature.

## Pin Configuration - 256K x 36



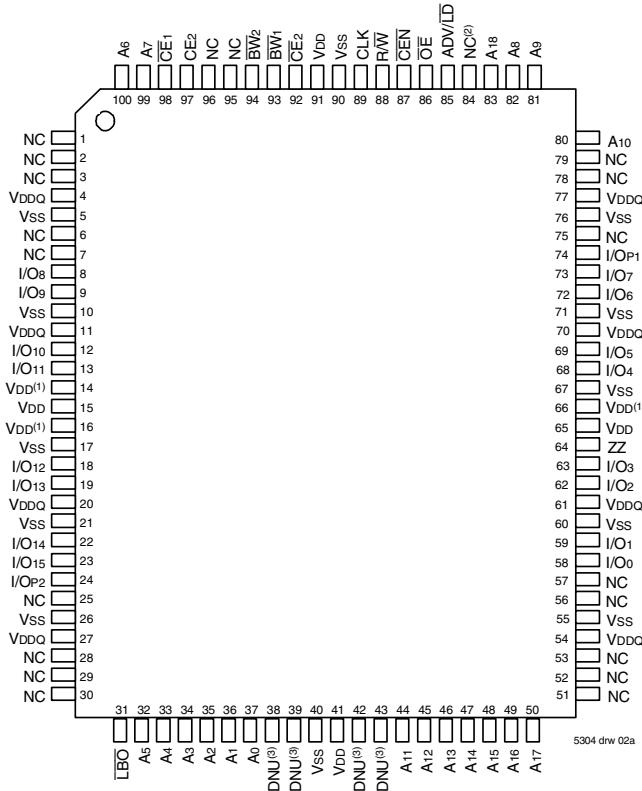
5304 drw 02

## Top View 100 TQFP

**NOTES:**

1. Pins 14, 16 and 66 do not have to be connected directly to VDD as long as the input voltage is <math>V\_{IH}</math>.
2. Pin 84 is reserved for a future 16M.
3. DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW (V<sub>ss</sub>), or tied HIGH (V<sub>DD</sub>).

## Pin Configuration - 512K x 18



### Top View 100 TQFP

#### NOTES:

- Pins 14, 16 and 66 do not have to be connected directly to  $V_{DD}$  as long as the input voltage is  $\geq V_{IH}$ .
- Pin 84 is reserved for a future 16M.
- DNU=Do not use. Pins 38, 39, 42 and 43 are reserved for respective JTAG pins: TMS, TDI, TDO and TCK. The current die revision allows these pins to be left unconnected, tied LOW ( $V_{SS}$ ), or tied HIGH ( $V_{DD}$ ).

## 100 TQFP Capacitance<sup>(1)</sup>

( $T_A = +25^\circ C$ ,  $f = 1.0MHz$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 3dV$	5	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3dV$	7	pF

5304 tbl 07

## 119 BGA Capacitance<sup>(1)</sup>

( $T_A = +25^\circ C$ ,  $f = 1.0MHz$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 3dV$	7	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3dV$	7	pF

5304 tbl 07a

#### NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3,6)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{DD}$	V
$V_{TERM}^{(4,6)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V
$V_{TERM}^{(5,6)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{DDQ} + 0.5$	V
$T_A^{(7)}$	Commercial Operating Temperature	-0 to +70	$^\circ C$
		Industrial Operating Temperature	-40 to +85
TBIAS	Temperature Under Bias	-55 to +125	$^\circ C$
TSTG	Storage Temperature	-55 to +125	$^\circ C$
PT	Power Dissipation	2.0	W
$I_{OUT}$	DC Output Current	50	mA

#### NOTES:

5304 tbl 06

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- $V_{DD}$  terminals only.
- $V_{DDQ}$  terminals only.
- Input terminals only.
- I/O terminals only.
- This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed  $V_{DDQ}$  during power supply ramp up.
- During production testing, the case temperature equals  $T_A$ .

## 165 fBGA Capacitance<sup>(1)</sup>

( $T_A = +25^\circ C$ ,  $f = 1.0MHz$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 3dV$	TBD	pF
$C_{I/O}$	I/O Capacitance	$V_{OUT} = 3dV$	TBD	pF

5304 tbl 07b

### Synchronous Truth Table<sup>(1)</sup>

$\overline{CEN}$	R/ $\overline{W}$	Chip <sup>(5)</sup> Enable	ADV/ $\overline{LD}$	$\overline{BW}_x$	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D <sup>(7)</sup>
L	H	Select	L	X	External	X	LOAD READ	Q <sup>(7)</sup>
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) <sup>(2)</sup>	D <sup>(7)</sup>
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) <sup>(2)</sup>	Q <sup>(7)</sup>
L	X	Deselect	L	X	X	X	DESELECT or STOP <sup>(3)</sup>	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND <sup>(4)</sup>	Previous Value

5304 tbl 08

**NOTES:**

- L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care.
- When ADV/ $\overline{LD}$  signal is sampled high, the internal burst counter is incremented. The R/ $\overline{W}$  signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/ $\overline{W}$  signal when the first address is loaded at the beginning of the burst cycle.
- Deselect cycle is initiated when either ( $\overline{CE}_1$ , or  $\overline{CE}_2$  is sampled high or  $\overline{CE}_2$  is sampled low) and ADV/ $\overline{LD}$  is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
- When  $\overline{CEN}$  is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- To select the chip requires  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$ ,  $\overline{CE}_2 = H$  on these chip enables. Chip is deselected if any one of the chip enables is false.
- Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
- Q - Data read from the device, D - data written to the device.

### Partial Truth Table for Writes<sup>(1)</sup>

OPERATION	R/ $\overline{W}$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$ <sup>(3)</sup>	$\overline{BW}_4$ <sup>(3)</sup>
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/OP1) <sup>(2)</sup>	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/OP2) <sup>(2)</sup>	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/OP3) <sup>(2,3)</sup>	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/OP4) <sup>(2,3)</sup>	L	H	H	H	L
NO WRITE W	L	H	H	H	H

5304 tbl 09

**NOTES:**

- L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = Don't Care.
- Multiple bytes may be selected during the same cycle.
- N/A for X18 configuration.

### Interleaved Burst Sequence Table ( $\overline{LBO}=VDD$ )

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	1	0	0	1	0	0

5304 tbl 10

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

### Linear Burst Sequence Table ( $\overline{LBO}=VSS$ )

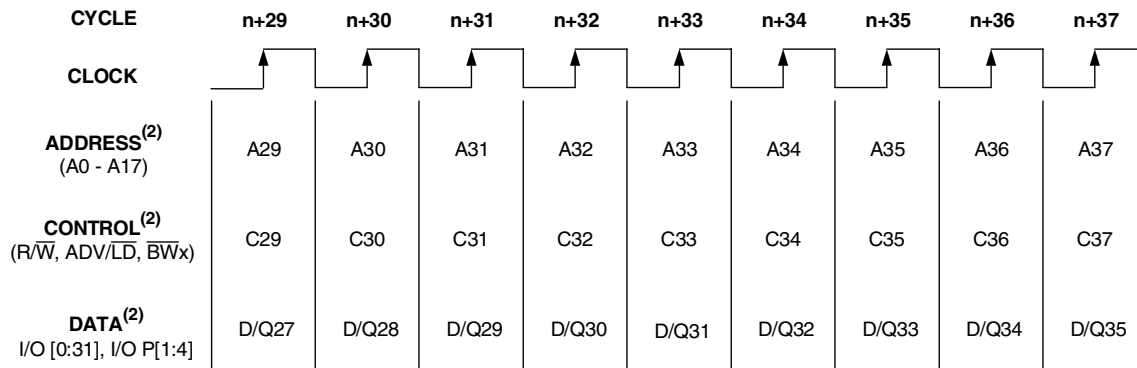
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address <sup>(1)</sup>	1	1	0	0	0	1	1	0

5304 tbl 11

**NOTE:**

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

### Functional Timing Diagram<sup>(1)</sup>



**NOTES:**

1. This assumes  $\overline{CEN}$ ,  $\overline{CE1}$ ,  $CE2$ ,  $\overline{CE2}$  are all true.
2. All Address, Control and Data\_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data\_Out is valid after a clock-to-data delay from the rising edge of clock.

5304 drw 03



## Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles<sup>(2)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(1)}$	$\overline{CEN}$	$\overline{BW}_x$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A <sub>1</sub>	H	L	L	L	X	L	Q <sub>0</sub>	Load read
n+3	X	X	L	H	L	X	L	Q <sub>0+1</sub>	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q <sub>1</sub>	NOOP
n+5	A <sub>2</sub>	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q <sub>2</sub>	Deselect or STOP
n+8	A <sub>3</sub>	L	L	L	L	L	L	Q <sub>2+1</sub>	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A <sub>4</sub>	L	L	L	L	L	X	D <sub>3</sub>	Load write
n+11	X	X	L	H	L	X	X	D <sub>3+1</sub>	Deselect or STOP
n+12	X	X	H	X	L	X	X	D <sub>4</sub>	NOOP
n+13	A <sub>5</sub>	L	L	L	L	L	X	Z	Load write
n+14	A <sub>6</sub>	H	L	L	L	X	X	Z	Load read
n+15	A <sub>7</sub>	L	L	L	L	L	X	D <sub>5</sub>	Load write
n+16	X	X	H	X	L	L	L	Q <sub>6</sub>	Burst write
n+17	A <sub>8</sub>	H	L	L	L	X	X	D <sub>7</sub>	Load read
n+18	X	X	H	X	L	X	X	D <sub>7+1</sub>	Burst read
n+19	A <sub>9</sub>	L	L	L	L	L	L	Q <sub>8</sub>	Load write

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### NOTES:

- $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .
- H = High; L = Low; X = Don't Care; Z = High Impedance.

## Read Operation<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BW}_x$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup and V
n+2	X	X	X	X	X	X	L	Q <sub>0</sub>	Contents of Address A <sub>0</sub> Read Out

### NOTES:

- H = High; L = Low; X = Don't Care; Z = High Impedance.
- $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

### Burst Read Operation<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q <sub>0+1</sub>	Address A <sub>0+1</sub> Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q <sub>0+2</sub>	Address A <sub>0+2</sub> Read Out, Inc. Count
n+5	A <sub>1</sub>	H	L	L	L	X	L	Q <sub>0+3</sub>	Address A <sub>0+3</sub> Read Out, Load A <sub>1</sub>
n+6	X	X	H	X	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q <sub>1</sub>	Address A <sub>1</sub> Read Out, Inc. Count
n+8	A <sub>2</sub>	H	L	L	L	X	L	Q <sub>1+1</sub>	Address A <sub>1+1</sub> Read Out, Load A <sub>2</sub>

**NOTES:**

1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2.  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

### Write Operation<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D <sub>0</sub>	Write to Address A <sub>0</sub>

**NOTES:**

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

### Burst Write Operation<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O	Comments
n	A <sub>0</sub>	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D <sub>0</sub>	Address A <sub>0</sub> Write, Inc. Count
n+3	X	X	H	X	L	L	X	D <sub>0+1</sub>	Address A <sub>0+1</sub> Write, Inc. Count
n+4	X	X	H	X	L	L	X	D <sub>0+2</sub>	Address A <sub>0+2</sub> Write, Inc. Count
n+5	A <sub>1</sub>	L	L	L	L	L	X	D <sub>0+3</sub>	Address A <sub>0+3</sub> Write, Load A <sub>1</sub>
n+6	X	X	H	X	L	L	X	D <sub>0</sub>	Address A <sub>0</sub> Write, Inc. Count
n+7	X	X	H	X	L	L	X	D <sub>1</sub>	Address A <sub>1</sub> Write, Inc. Count
n+8	A <sub>2</sub>	L	L	L	L	L	X	D <sub>1+1</sub>	Address A <sub>1+1</sub> Write, Load A <sub>2</sub>

**NOTES:**

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

### Read Operation with Clock Enable Used<sup>(1)</sup>

Cycle	Address	R/ $\bar{W}$	ADV/ $\bar{LD}$	$\bar{CE}^{(2)}$	$\bar{CEN}$	$\bar{BW}_x$	$\bar{OE}$	I/O	Comments
n	A <sub>0</sub>	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A <sub>1</sub>	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q <sub>0</sub>	Clock Ignored, Data Q <sub>0</sub> is on the bus.
n+4	X	X	X	X	H	X	L	Q <sub>0</sub>	Clock Ignored, Data Q <sub>0</sub> is on the bus.
n+5	A <sub>2</sub>	H	L	L	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read out (bus trans.)
n+6	A <sub>3</sub>	H	L	L	L	X	L	Q <sub>1</sub>	Address A <sub>1</sub> Read out (bus trans.)
n+7	A <sub>4</sub>	H	L	L	L	X	L	Q <sub>2</sub>	Address A <sub>2</sub> Read out (bus trans.)

**NOTES:**

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\bar{CE} = L$  is defined as  $\bar{CE}_1 = L$ ,  $\bar{CE}_2 = L$  and  $CE_2 = H$ .  $\bar{CE} = H$  is defined as  $\bar{CE}_1 = H$ ,  $\bar{CE}_2 = H$  or  $CE_2 = L$ .

### Write Operation with Clock Enable Used<sup>(1)</sup>

Cycle	Address	R/ $\bar{W}$	ADV/ $\bar{LD}$	$\bar{CE}^{(2)}$	$\bar{CEN}$	$\bar{BW}_x$	$\bar{OE}$	I/O	Comments
n	A <sub>0</sub>	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A <sub>1</sub>	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A <sub>2</sub>	L	L	L	L	L	X	D <sub>0</sub>	Write Data D <sub>0</sub>
n+6	A <sub>3</sub>	L	L	L	L	L	X	D <sub>1</sub>	Write Data D <sub>1</sub>
n+7	A <sub>4</sub>	L	L	L	L	L	X	D <sub>2</sub>	Write Data D <sub>2</sub>

**NOTES:**

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2.  $\bar{CE} = L$  is defined as  $\bar{CE}_1 = L$ ,  $\bar{CE}_2 = L$  and  $CE_2 = H$ .  $\bar{CE} = H$  is defined as  $\bar{CE}_1 = H$ ,  $\bar{CE}_2 = H$  or  $CE_2 = L$ .

## Read Operation with Chip Enable Used<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O <sup>(3)</sup>	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A <sub>0</sub>	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A <sub>1</sub>	H	L	L	L	X	L	Q <sub>0</sub>	Address A <sub>0</sub> Read out. Load A <sub>1</sub> .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q <sub>1</sub>	Address A <sub>1</sub> Read out. Deselected.
n+7	A <sub>2</sub>	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q <sub>2</sub>	Address A <sub>2</sub> Read out. Deselected.

### NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

## Write Operation with Chip Enable Used<sup>(1)</sup>

Cycle	Address	R/W	ADV/LD	$\overline{CE}^{(2)}$	$\overline{CEN}$	$\overline{BWx}$	$\overline{OE}$	I/O <sup>(3)</sup>	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A <sub>0</sub>	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A <sub>1</sub>	L	L	L	L	L	X	D <sub>0</sub>	Address D <sub>0</sub> Write in. Load A <sub>1</sub> .
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D <sub>1</sub>	Address D <sub>1</sub> Write in. Deselected.
n+7	A <sub>2</sub>	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D <sub>2</sub>	Address D <sub>2</sub> Write in. Deselected.

### NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2.  $\overline{CE} = L$  is defined as  $\overline{CE}_1 = L$ ,  $\overline{CE}_2 = L$  and  $CE_2 = H$ .  $\overline{CE} = H$  is defined as  $\overline{CE}_1 = H$ ,  $\overline{CE}_2 = H$  or  $CE_2 = L$ .

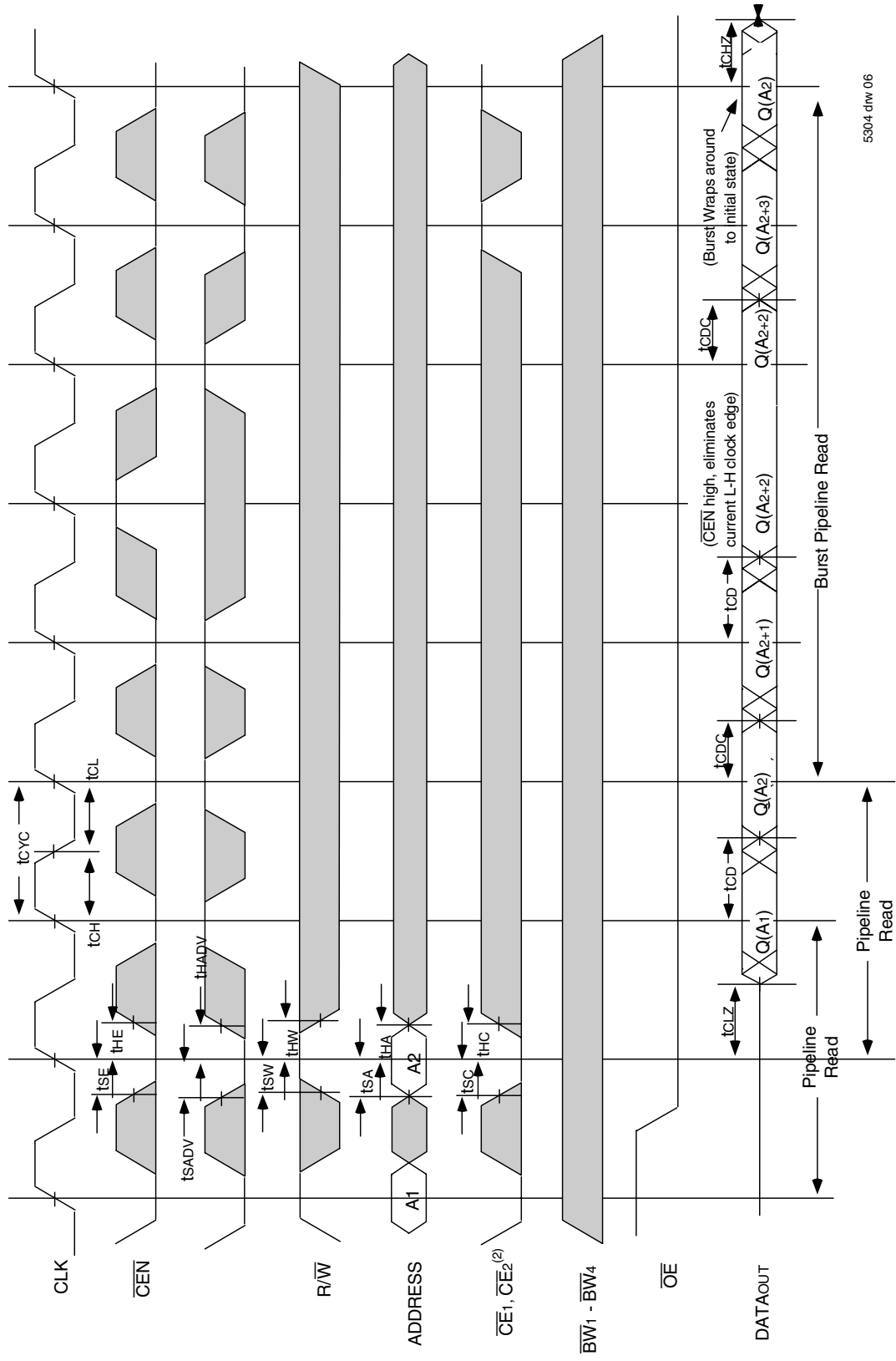
## AC Electrical Characteristics (VDD = 3.3V +/-5%, Industrial Temperature Range)

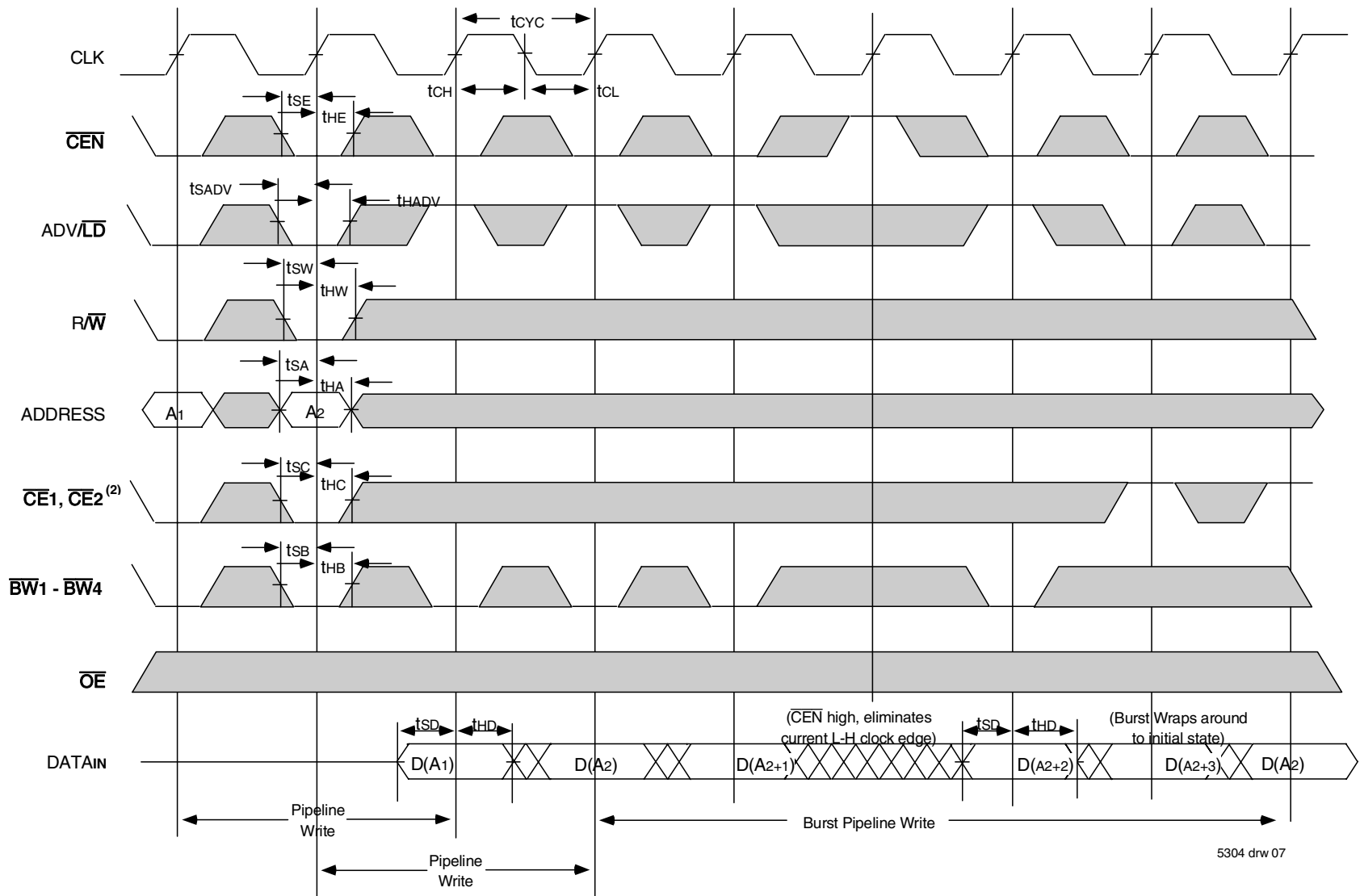
Symbol	Parameter	150MHz		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Clock Cycle Time	6.7	—	7.5	—	10	—	ns
t <sub>F</sub> <sup>(1)</sup>	Clock Frequency	—	150	—	133	—	100	MHz
t <sub>CH</sub> <sup>(2)</sup>	Clock High Pulse Width	2.0	—	2.2	—	3.2	—	ns
t <sub>CL</sub> <sup>(2)</sup>	Clock Low Pulse Width	2.0	—	2.2	—	3.2	—	ns
<b>Output Parameters</b>								
t <sub>CD</sub>	Clock High to Valid Data	—	3.8	—	4.2	—	5	ns
t <sub>DC</sub>	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
t <sub>CLZ</sub> <sup>(3,4,5)</sup>	Clock High to Output Active	1.5	—	1.5	—	1.5	—	ns
t <sub>CHZ</sub> <sup>(3,4,5)</sup>	Clock High to Data High-Z	1.5	3	1.5	3	1.5	3.3	ns
t <sub>OE</sub>	Output Enable Access Time	—	3.8	—	4.2	—	5	ns
t <sub>OLZ</sub> <sup>(3,4)</sup>	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(3,4)</sup>	Output Enable High to Data High-Z	—	3.8	—	4.2	—	5	ns
<b>Set Up Times</b>								
t <sub>SE</sub>	Clock Enable Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SA</sub>	Address Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SD</sub>	Data In Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SW</sub>	Read/Write (R/ $\bar{W}$ ) Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SADV</sub>	Advance/Load (ADV/ $\bar{LD}$ ) Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SC</sub>	Chip Enable/Select Setup Time	1.5	—	1.7	—	2.0	—	ns
t <sub>SB</sub>	Byte Write Enable ( $\bar{B}\bar{W}$ x) Setup Time	1.5	—	1.7	—	2.0	—	ns
<b>Hold Times</b>								
t <sub>HE</sub>	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HD</sub>	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HW</sub>	Read/Write (R/ $\bar{W}$ ) Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HADV</sub>	Advance/Load (ADV/ $\bar{LD}$ ) Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HC</sub>	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>HB</sub>	Byte Write Enable ( $\bar{B}\bar{W}$ x) Hold Time	0.5	—	0.5	—	0.5	—	ns

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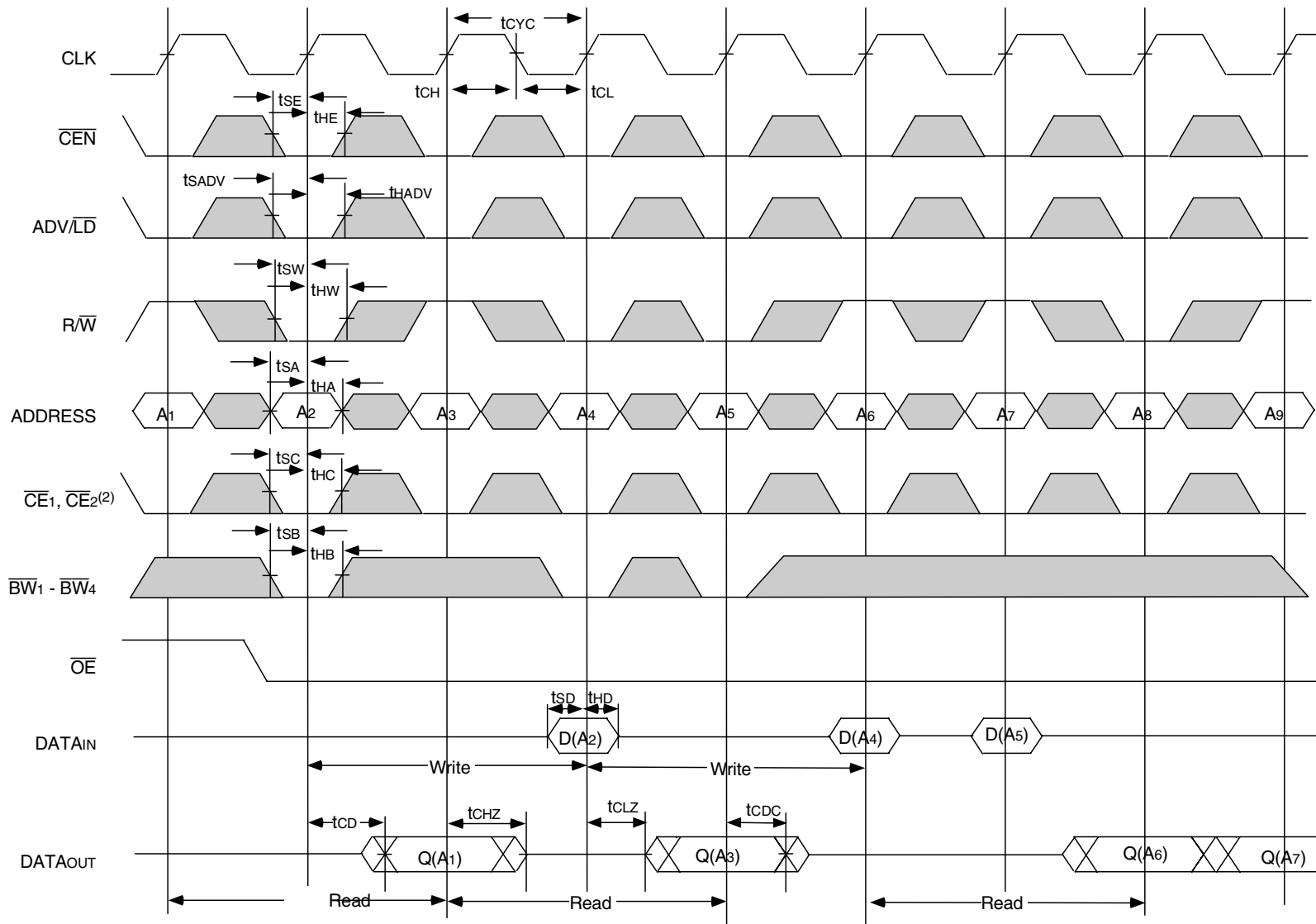
### NOTES:

- t<sub>F</sub> = 1/t<sub>CYC</sub>.
- Measured as HIGH above 0.6V<sub>DDQ</sub> and LOW below 0.4V<sub>DDQ</sub>.
- Transition is measured ±200mV from steady-state.
- These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
- To avoid bus contention, the output buffers are designed such that t<sub>CHZ</sub> (device turn-off) is about 1ns faster than t<sub>CLZ</sub> (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t<sub>CLZ</sub> is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t<sub>CHZ</sub>, which is a Max. parameter (worse case at 70 deg. C, 3.135V).





# Timing Waveform of Combined Read and Write Cycles (1,2,3)

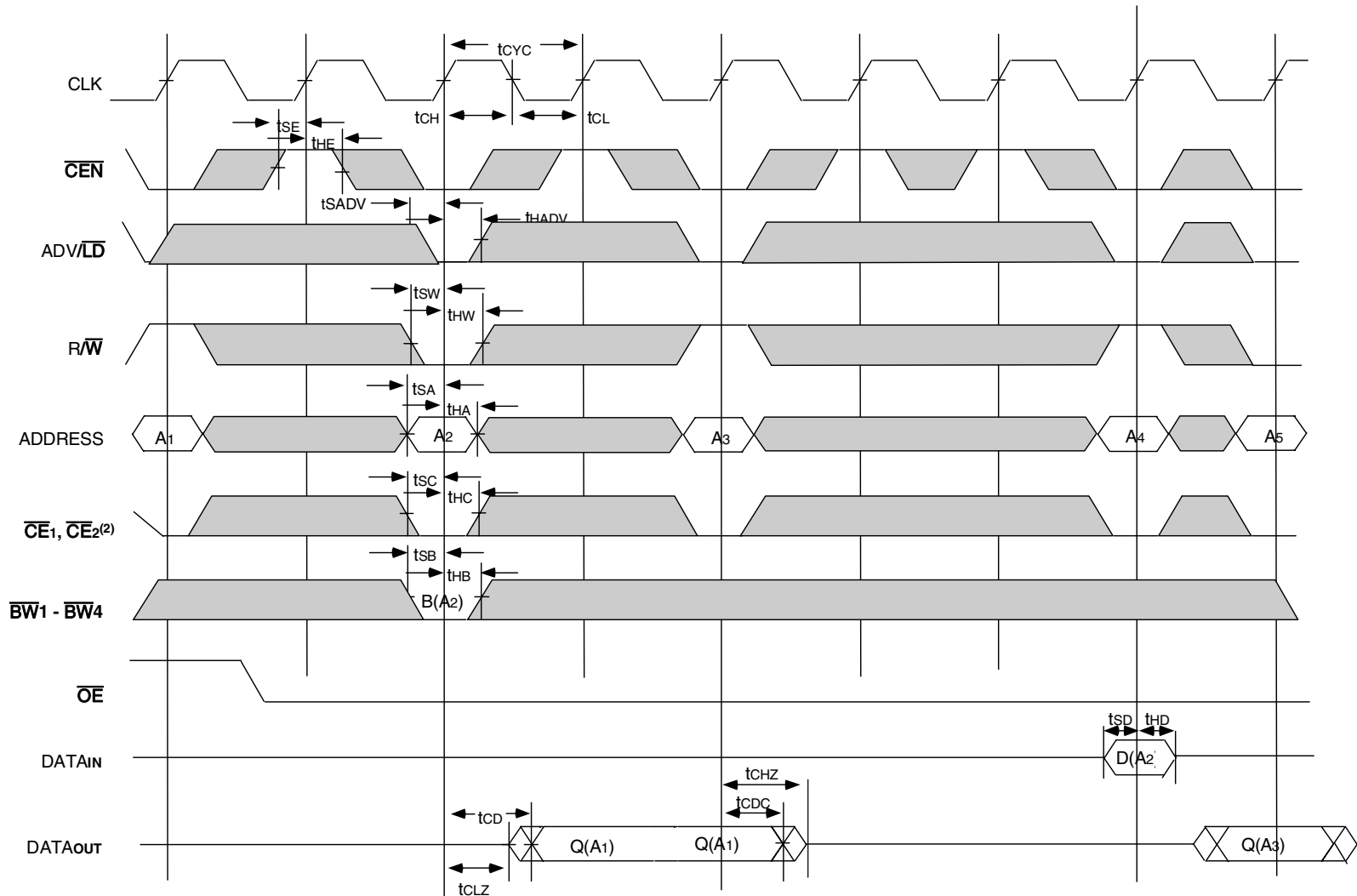


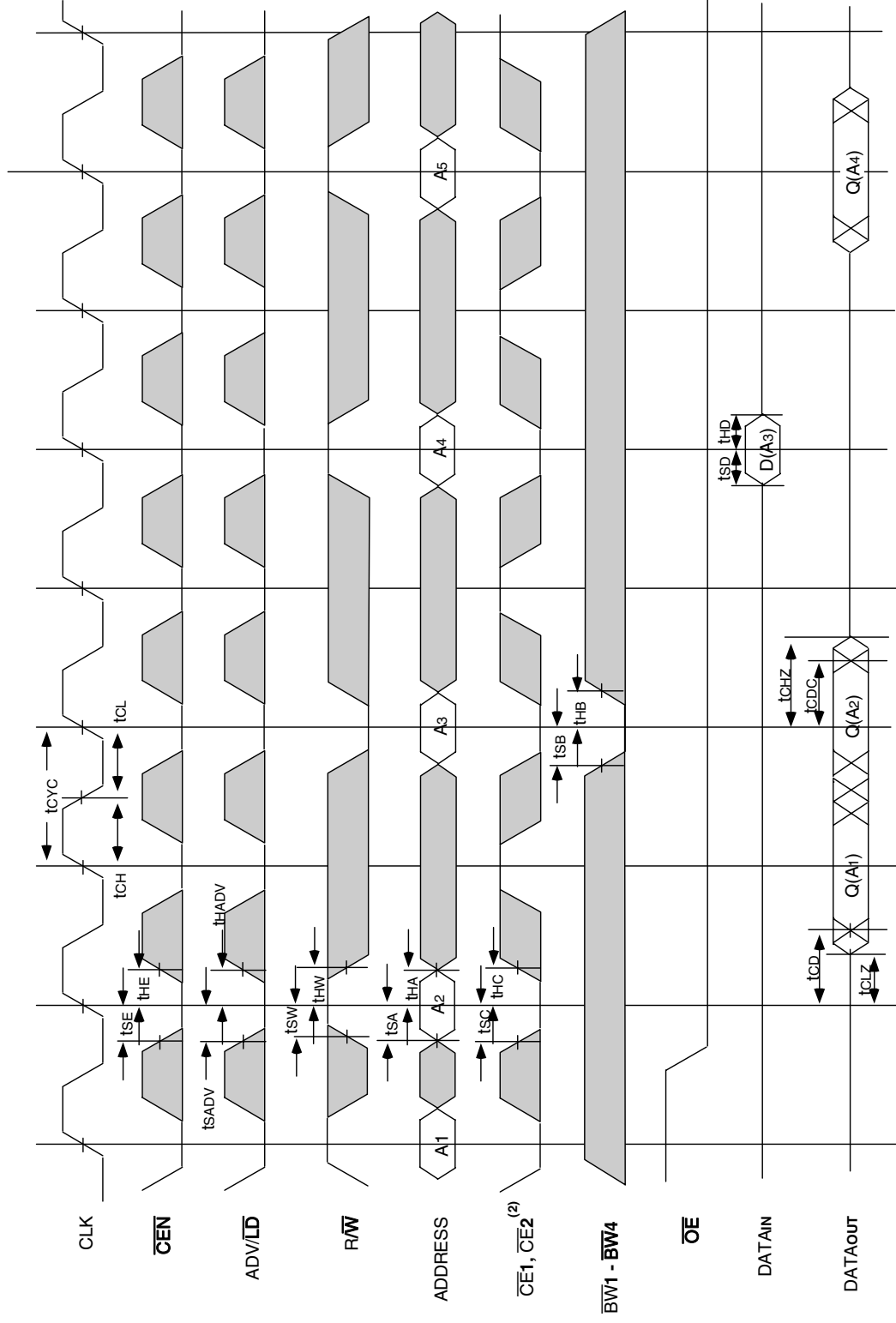
5304 drw 08

### NOTES:

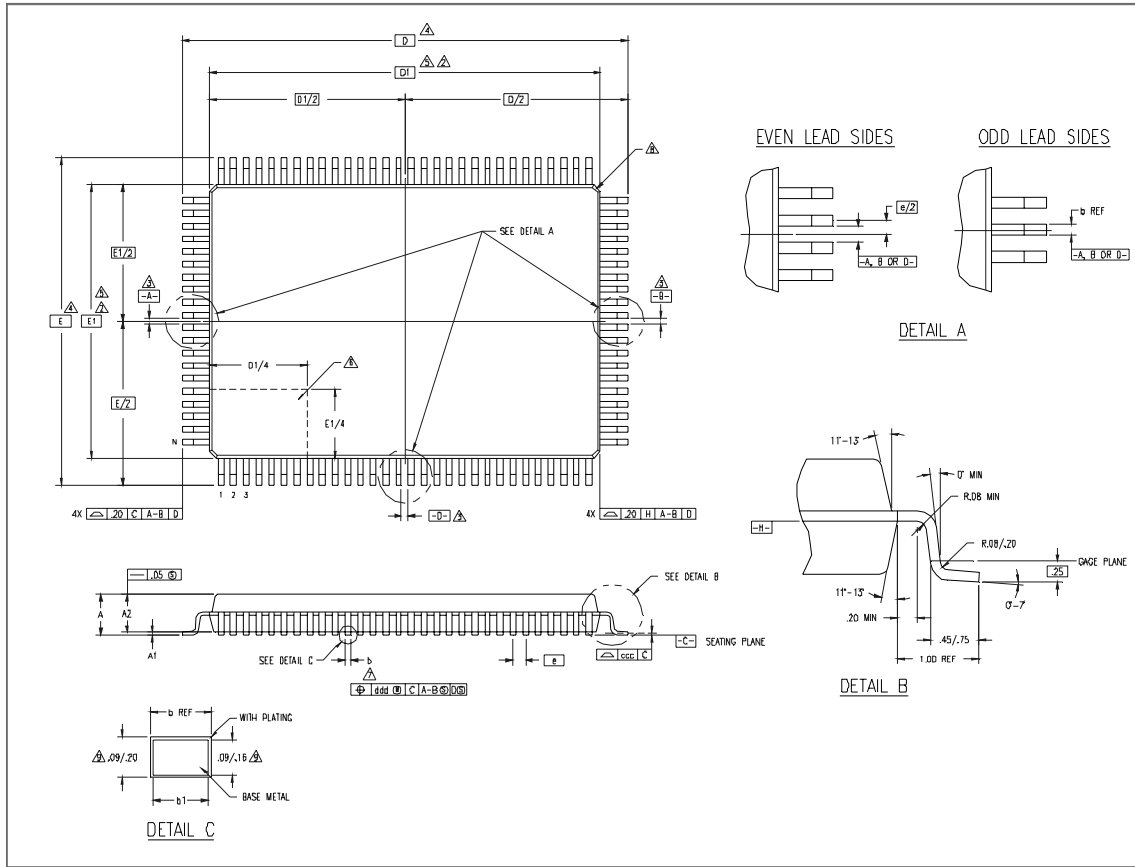
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals ( $\overline{BW}_x$ ) must be valid on all write and burst-write cycles. A write cycle is initiated when  $\overline{R/W}$  signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.





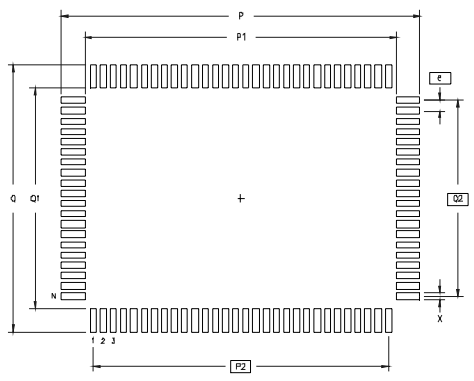


# 100-Pin Plastic Thin Quad Flatpack (TQFP) Package Diagram Outline



SYMBOL	JEDEC VARIATION			N
	MIN	NGM	MAX	
A			1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D	22.00 BSC			4
D1	20.00 BSC			5,2
E	16.00 BSC			4
E1	14.00 BSC			5,2
N	100			
ND	3D			
NE	2D			
e	.65 BSC			
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	-	-	.10	
ddd	-	-	.13	

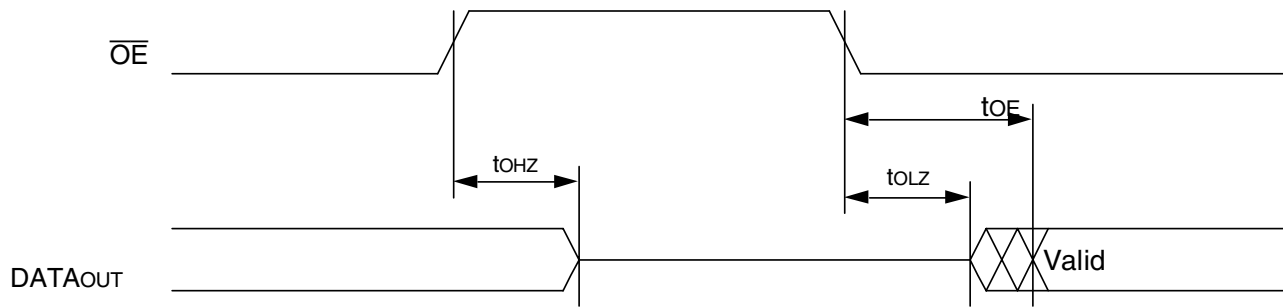
## LAND PATTERN DIMENSIONS



	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85	BSC
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35	BSC
X	.30	.50
e	.65 BSC	
N	100	

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- △ DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION, ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- △ DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

## Timing Waveform of $\overline{OE}$ Operation<sup>(1)</sup>



**NOTE:**

1. A read operation is assumed to be in progress.

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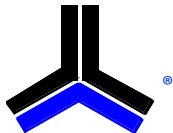
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## ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed Mhz
AS8C803601-QC150N	256K x 36	3.1 - 3.4V	100 pin TQFP	Comercial 0 - 70C	150
AS8C801801-QC150N	512K x 18	3.1 - 3.4V	100 pin TQFP	Comercial 0 - 70C	150

## PART NUMBERING SYSTEM

AS8C	Device	Conf.	Mode	Package	Operating Temp	Speed	N
Sync. SRAM prefix	80 = 8M	18= x18 36 = x36	01= ZBT 00 = Pipelined 25 = Flow- Thru	Q = 100 Pin TQFP	0 ~ 70C	150MHz	N= Leadfree



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Document Version: v. 1.0

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